IN THE SPECIFICATION

Please add the following paragraphs on page 6, line 11.

Figures 4A-4K illustrate an embodiment of a process of fabrication of a transistor according to the teachings of the present invention.

Figures 5A-5C illustrate an additional embodiment of the process of fabrication taught in connection with Figures 4A-4K.

Figures 6A-6O illustrate an embodiment of a process of fabrication of a complementary pair of transistors according to the teachings of the present invention.

Figure 7 is a perspective view of an embodiment of an array transistors formed according to the method of Figures 4A-4K and Figures 5A-5C.

Figure 8 is a perspective view of an embodiment of transistor formed according to the method of Figures 6A-6O.

Figure 9 is a planar view of an embodiment of a dual-gated transistor according to the teachings of the present invention.

Please add the following paragraphs on page 11, line 24, before the Conclusion.

Figures 4A-4K illustrate an embodiment of a process of fabrication of a transistor according to the teachings of the present invention. In the embodiment of Figure 4A, a p- bulk silicon substrate 510 starting material is used. An n++ and n+ silicon composite first source/drain layer 512 is formed on substrate 510, such as by ion-implantation, epitaxial growth, or a combination of such techniques. The overall thickness of the first source/drain layer 512 can be approximately between 0.2 to 0.5 μm. A body region layer 514 of p- silicon is formed, such as by vertical epitaxial growth, to a thickness that can be about 0.4 μm. A second source/drain region layer 516 of n+ silicon is formed, such as by ion-implantation into body region layer 514 or by epitaxial growth on body region layer 514, to a thickness that can be approximately between 0.2 and 0.5 μm.

In an alternative embodiment the approximate thicknesses provided above for the first source/drain region layer 512, the body region layer 514, and the second source/drain region

layer 516 can be proportionally scaled down to provide a sub-micron device which has a body region layer 514 thickness of less than 0.5 μm.

In Figure 4B, a silicon dioxide (SiO_2) thin pad oxide layer 812 is formed on second source/drain region 516, such as by chemical vapor deposition (CVD). In one embodiment, pad oxide layer 812 can be approximately 10 nm in thickness. A thin silicon nitride (Si_3N_4) layer 814 is formed on pad oxide layer 812, such as by CVD. In one embodiment, nitride layer 814 can be approximately 100 nm in thickness.

In Figure 4C, photoresist is applied and selectively exposed to provide a mask for the directional etching of trenches 520, such as by reactive ion etching (RIE). The directional etching results in a plurality of column bars 816 containing the stack of nitride layer 814, pad oxide layer 812, second source/drain layer 516, body region layer 514, and first source/drain layer 512. Trenches 520 are etched to a depth that is sufficient to reach the surface 818 of substrate 510, thereby providing separation between what can serve as conductively doped bit lines 502 beneath the first source/drain region layer 512. Bars 816 are oriented in the direction of bit lines 502. In an exemplary embodiment, bars 816 have a surface line width which is sufficiently thin, vis-a-vis the doping concentration of the body region 514, such that the bulk charge is extremely small, negligible in device operation, and the body region 514 can be fully depleted when a gate potential is applied. The depth and width of each trench 520 can be approximately equal to the line width of bars 816.

In Figure 4D, the photoresist is removed. Isolation material 524, such as SiO_2 is deposited to fill the trenches 520. The working surface is then planarized, such as by chemical mechanical polishing/planarization (CMP).

Figure 4E illustrates the view of Figure 1D after clockwise rotation by ninety degrees. In Figure 4E, a photoresist material is applied and selectively exposed to provide a mask for the directional etching of trenches 521 and 522, such as by reactive ion etching (RIE) of a plurality of row bars 832 that are disposed orthogonally to bit lines 502. Forming trenches 521 and 522 includes etching though stacked layers in the portions of bars 816. Forming trenches 521 and 522 also includes etching through the isolation material 524 disposed between bars 816.

More particularly, trenches 521 and 522 are etched through nitride layer 814, pad oxide layer 812, second source/drain layer 516, body region layer 514, and partially into first

source/drain layer 512. Trenches 521 and 522 are etched into bars 816 to a sufficient depth into first source/drain layer 512 such that the underlying bit line 502 portion of the first source/drain layer 512 is left intact. Trenches 521 and 522 are also etched into the isolation material 524 between bars 816. In one embodiment, after etching nitride layer 814 of bars 816, a nonselective dry etch is used to remove the isolation material 524 between bars 816 and also the pad oxide layer 812, second source/drain layer 516, body region layer 514, and a portion of first source/drain layer 512 of bars 816. The directional etching of trenches 521 and 522 results in the formation of a plurality of row bars 832 that are orthogonal to column bars 816.

Figure 4F is a plan view illustrating generally the arrangement of parallel bars 816, and trenches 520 interposed therebetween. Bars 832 are arranged orthogonally to bars 816. Trenches 521 and 522 are interposed between ones of bars 832. The resulting semiconductor pillars in the intersecting portions of bars 832 and 816 provide first and second source/drain regions 512 and 516, respectively, and body region 514 for metal-oxide semiconductor field effect transistor (MOSFET) formation.

In Figure 4G, which is oriented similarly to Figure 4E, a conformal silicon nitride layer 840 is formed, such as by CVD. Nitride layer 840 is directionally etched, such as by RIE, to leave resulting portions of nitride layer 840 only on the first and second opposing sidewalls, 519A and 519B, of the bars 832 in trenches 521 and 522. In one embodiment, the thickness of nitride layer 840 is about 20 nm. An oxide layer 842 is formed, such as by thermal growth, at the base portions of trenches 521 and 522. Oxide layer 842 insulates the underlying bit lines 502 from structures subsequently formed in trenches 521 and 522. After forming oxide layer 842, remaining portions of nitride layer 840 are removed.

In Figure 4H, a gate oxide 518 is formed on the first and second opposing sidewalls, 519A and 519B, in trenches 521 and 522 of second source/drain region 516, body region 514, and first source/drain region 512. In one embodiment, gate oxide 518 is a high-quality thin oxide layer that is thermally grown on the first and second opposing sidewalls, 519A and 519B, of trenches 521 and 522.

In Figure 4I, a conductive layer 844 is formed over the working surface of the wafer, including filling trenches 521 and 522 in which respective first and second word lines 506 and 508 will be formed. The first and second word lines 506 and 508 will serve as first and second

gates, 506 and 508, opposing the first and second opposing sidewalls, 519A and 519B, of trenches 521 and 522. In one embodiment, layer 844 is formed by CVD of a refractory metal, such as tungsten. In another embodiment, layer 844 is formed by CVD of n+ polysilicon.

In Figure 4J, CMP or other suitable planarization process is used to remove portions of layer 844 above the interface between pad oxide 812 and second source/drain layer 516. Pad oxide 812 and nitride layer 814 are also removed during this planarization step. As a result of the planarization step, first and second word lines 506 and 508, which serve as first and second gates, 506 and 508, opposing the first and second opposing sidewalls, 519A and 519B, are formed in trenches 521 and 522.

In Figure 4K, the first and second gates, 506 and 508, opposing the first and second opposing sidewalls, 519A and 519B are directionally etched, thereby leaving resulting separate gates 506A, 506B and 508A, 508B. In one embodiment, separate gates 506A and 508B serve as a first gate 506A and second gate 508B opposing the first and second opposing sidewalls, 519A and 519B, in trenches 521 and 522. Splitting the first and second gates, 506 and 508, respectively, provides the resulting structure illustrated in Figure 7, but is not required to practice the invention. In one embodiment, an insulating layer 846, such as SiO_2, is formed on the working surface of the wafer, such as by CVD. The structure thus formed may undergo further processing steps to complete integrated circuits on the working surface of the wafer using known techniques and followed by conventional back end of line (BEOL) procedures.

Figures 5A-5C illustrate generally, by way of example, additional steps used to form SOI bars during the fabrication steps described above with respect to Figures 4A-4K, such that the MOSFET formed, extends vertically outward from an insulating portion 902 of substrate 510.

In Figure 5A, the processing steps described above with respect to Figures 4A-4C are carried out, forming trenches 520 that are etched to a depth that is below the original surface 818 of substrate 510, such as by approximately greater than or equal to 0.6 μm. A nitride layer 1004 is formed, such as by CVD. Nitride layer 1004 is directionally etched, such as by RIE, to remove nitride layer 704 from the base regions of trenches 520. Portions of nitride layer 1004 remain on the sidewall of trenches 520 to protect adjacent layers during subsequent etching and oxidation.

In Figure 5B, an isotropic chemical etch of silicon is used to partially undercut bars 816. For example, hydrofluoric acid (HF) or a commercial etchant sold under the trade name CP4 (a mixture of approximately 1 part (46% HF):1 part (CH_3COOH):3 parts (HNO_3)) can be used for the isotropic etchant. In one embodiment, the partial undercutting of bars 816 by isotropic etching is timed to remove a volume of silicon that is sufficient to compensate for a subsequently formed volume of oxide, described below. In general, the subsequent oxidation step produces a volume of oxide that is approximately twice that of the silicon consumed during oxidation.

In Figure 5C, substrate 510 is oxidized using a standard semiconductor processing furnace at a temperature of approximately 900 to 1,100 degrees Celsius. A wet oxidizing ambient is used in the furnace chamber to oxidize the exposed silicon regions in the lower portion of trenches 520. Substrate 510 is oxidized for a time period that is sufficient to form oxide insulating portion 902 that fully undercuts bars 816. Insulating portion 902 underlies both bars 816 and trenches 520, and isolates the bit lines 502 and MOSFETs formed on bit lines 502 from an underlying semiconductor portion of substrate 510. Nitride layer 1004 is removed, and processing then continues as described above with respect to Figures 4D-4K.

In one embodiment, bars 816 are sufficiently narrow such that the oxidation step that undercuts bars 816 produces sufficient oxide to fill trenches 520, resulting in a generally planar structure. This avoids the need for a separate step of depositing an oxide insulation material 524 described with respect to Figure 4D. The oxidation time period depends on the width of bars 816 and the effective width of bars 816 after the undercut etch step. Narrower bars 816 require shorter oxidation times. For example, for sub-0.25 micron technology, oxidation time is approximately 1 hour. In another embodiment, the etch step fully undercuts bars 816 before oxidation. This further reduces oxidation time.

Figures 6A-6O illustrate an embodiment of a process of fabrication of a complementary pair of transistors according to the teachings of the present invention. Figure 6A begins with a lightly doped p– silicon substrate 700. A thin screen oxide layer 702 is thermally grown. The oxide layer 702 is formed to a thickness of approximately 10 nanometers (nm). A photoresist is applied and selectively exposed to reveal p-channel metal-oxide semiconductor (PMOS) device regions 705. Wells of n-type silicon material are formed in the substrate 700 to form the PMOS device regions 705. The n-wells 710 of n-type material can be formed by any suitable method,

such as by ion implantation. The n-wells 710 are formed to a depth of approximately 1.0 micrometer (μm). The photoresist is removed using conventional photoresist stripping techniques. The structure is then annealed, such as by a rapid thermal anneal (RTA) process, to achieve the desired doping profile. The structure is now as it appears in Figure 6A.

Figure 6B illustrates the structure after the next sequence of processing steps. A silicon nitride (Si_3N_4) pad layer 711 is deposited on the upper surface 704 of the substrate 700 and the n-wells 710. The nitride layer 711 is formed by any suitable means, such as by chemical vapor deposition (CVD). The nitride layer 711 is formed to a thickness of approximately 0.4 μm. A photoresist is applied and selectively exposed to mask stripes which define active device regions, including both n-channel metal-oxide semiconductor (NMOS) device regions 707 and PMOS device regions 705. In an exemplary embodiment, the active device regions, including both n-channel metal-oxide semiconductor (NMOS) device regions 707 and PMOS device regions 705 are defined to have a width which is sufficiently thin, vis-a-vis the doping concentration of the body region 514, such that the bulk charge in the active device regions is extremely small, negligible in device operation. This is to facilitate that the active device regions, including both n-channel metal-oxide semiconductor (NMOS) device regions 707 and PMOS device regions 705 can be fully depleted when a gate potential is applied. The nitride layer 711 in between device regions, 705 and 707, is removed. The nitride layer 711 is removed by any suitable etching technique, such as by RIE. The exposed n-well material 710 and p– substrate material 700 is etched to a depth of approximately 0.2 μm below the bottom of the n-well 710/substrate 700 interface. These etching steps leave trenches 714 between the device regions 707 and 705. The etching is performed though any suitable process, such as by RIE. The structure is now as shown in Figure 6B. The photoresist is next stripped, using conventional photoresist stripping techniques.

Figure 6C illustrates the structure after the next series of processing steps. An insulator layer 715 is formed beneath the device regions, 705 and 707 respectively, so as to form a semiconductor on insulator (SOI) structure. The insulator layer 715 is formed using, for example, the techniques of U.S. Application Serial No. 08/745,708, entitled *Silicon-On-Insulator Islands and Method for Their Formation* (the '708 Application), or U.S. Patent No. 5,691,230, entitled *Technique for Producing Small Islands of Silicon on Insulator* (the '230 Patent). The

'708 Application and the '230 Patent are incorporated by reference. The insulator layer 715 separates from substrate 700 the p– single crystalline silicon structure 712 of the NMOS device region 707, and the single crystalline silicon structure n-well 710 of the PMOS device region 705. Any of the nitride layer 711 left on the device regions, 705 and 707, is removed by etching. Any suitable etching technique may be used. In one embodiment, the nitride layer is removed by reactive ion etching (RIE). In an alternative embodiment, the nitride layer is removed using a wet etch process. The structure is now as illustrated in Figure 6C.

Figure 6D illustrates the structure following the next series of processing steps. A thin oxide layer 720 is thermally grown on active device regions, 705 and 707. The oxide layer 720 is grown to a thickness of approximately 20 nanometers (nm). A thin silicon nitride (Si_3N_4) layer 725 is deposited over the entire surface by CVD. The nitride layer 725 is deposited to a thickness of approximately 50 nm. Intrinsic polysilicon 730 is deposited by any suitable methods, such as by CVD, to fill the trenches 714. Next, the intrinsic polysilicon 730 over the structure is planarized stopping on the nitride pads 725. The intrinsic polysilicon 730 can be planarized by any suitable process, such as by chemical mechanical polishing/planarization (CMP). The intrinsic polysilicon 730 in the trenches 714 is selectively etched back further, such as by RIE, to leave only a thin layer on the bottom of trenches 714. The structure is now as is shown in Figure 6D.

Figure 6E shows the structure following the next sequence of processing steps. Every exposed portion of the nitride layer 725 is removed by a selective wet etch or RIE, leaving only the nitride 725 covered by the intrinsic polysilicon 730 at the bottom of the trenches 714. The intrinsic polysilicon 730 is then removed by a selective wet etch or RIE. The device regions, 705 and 707 respectively, remain protected by the oxide layer 720. Next, n-doped glass 732 is deposited, such as by CVD. In one embodiment the n-doped glass 732 is Arsenic silicate glass (ASG). In another embodiment, the n-doped glass 732 is Phosphorus silicate glass (PSG). The n-doped glass 732 is deposited to a thickness of approximately 100 nm. A new silicon nitride (Si_3N_4) layer 734 is deposited over the n-doped glass 732. The new nitride layer 734 is CVD deposited to a thickness of approximately 20 nm. A photoresist is applied and selectively exposed to reveal PMOS device regions 705 and to pattern the n-doped glass 732 in the NMOS

device regions 707 in the form of future first and second source/drain regions. The structure is now as is shown in Figure 6E.

Figure 6F illustrates the structure following the next series of process steps. The exposed nitride 734 and the underlying n-doped glass 732 are removed by any suitable means, such as by RIE. The nitride located at the bottom of the trenches 714 serves as an etch stop and protects the underlying insulator layer 715. The photoresist is stripped using conventional stripping techniques. A thin nitride layer 734 remains on the patterned n-doped glass 732 which was shielded by the photoresist. The structure is now as is shown in Figure 6F.

Figure 6G illustrates the structure following the next sequence of steps. A p-doped glass 736 is deposited by any suitable means such as, for example, CVD. In one embodiment, the p-doped glass 736 is borosilicate glass (BSG). The p-doped glass 736 is deposited to a thickness of approximately 100 nm. Again, a photoresist is applied and exposed to now reveal the NMOS device regions 707 and to pattern the p-doped glass 736 in the PMOS device regions 705 in the form of future first and second source/drain regions. The structure is now as is shown in Figure 6G.

Figure 6H illustrates the structure following the next series of process steps. The exposed p-doped glass 736 is removed by any suitable means, such as by RIE. The nitride located at the bottom of the trenches 714 again serves as an etch stop and protects the underlying insulator layer 715. Also, the thin nitride layer 734 remaining on patterned n-doped glass 732 portions serves as an etch stop and protects the regions of patterned n-doped glass 732. The photoresist is stripped using conventional stripping techniques. The structure is now as shown in Figure 6H.

Figure 6I provides a perspective view of the structure after the next process step. In this step a gate oxide 750 is thermally grown on the p– single crystalline silicon structure 712 of the NMOS device region 707, and on the n-well single crystalline silicon structure 710 of the PMOS device region 705.

Figure 6J carries the sequence of process steps further. In Figure 6J, a thin intrinsic polysilicon layer 755 is deposited, such as by CVD. The intrinsic polysilicon layer 755 is formed to a thickness of approximately 50 nm. Next, a thin oxide layer 756 is deposited on the intrinsic polysilicon layer 755. The oxide layer 756 can be deposited by any suitable method, such as by CVD. The oxide layer is deposited to a thickness of approximately 10 nm. A

photoresist is applied and masked to expose the NMOS device region 707. The exposed oxide layer 756 is etched back. The etching is performed by any suitable method and can be accomplished using reactive ion etching (RIE). The structure is now as appears in Figure 6J.

Figure 6K illustrates the structure following the next sequence of process steps. Figure 6K is a cross-sectional view of the gate region 709 taken along cut line 6K-6K. The photoresist has been stripped using conventional photoresist stripping techniques. Now, an n+ polysilicon layer 760 is deposited across the entire surface. The n+ polysilicon layer is deposited by any suitable means, such as by CVD. Next, a nitride layer 761 is deposited across the entire surface, such as by CVD. The nitride layer is deposited to a thickness of approximately 20 nm. A photoresist is applied and selectively exposed to reveal the PMOS device regions 705. The exposed nitride layer 761 and n+ polysilicon layer 760 underneath are etched off, such as by RIE. The exposed oxide layer 756 is next etched away by RIE. The structure is now as appears in Figure 6K.

Figure 6L illustrates the structure following the next sequence of process steps. The photoresist has been stripped using conventional photoresist stripping techniques. Now, a p+ polysilicon layer 762 is deposited across the entire surface. The p+ polysilicon layer is deposited by any suitable means, such as by CVD. A photoresist is applied and selectively exposed to reveal the NMOS device regions 707. The exposed p+ polysilicon layer 762 is etched off, such as by RIE. The structure is now as appears in Figure 6L.

Figure 6M illustrates the structure after the next group of process steps. The photoresist is stripped using conventional photoresist stripping techniques. The structure undergoes an anneal, such as a rapid thermal anneal (RTA), in order to drive the dopant species from the heavily doped n+ and p+ polysilicon layer, 760 and 762 respectively, into the underlying, undoped polysilicon 755. This step forms a heavily doped n+ gate layer 763 in the NMOS device region 707, and forms a heavily doped p+ silicon gate layer 764 in the PMOS device region 705. The anneal also serves to drive the dopant into the n-well single crystalline silicon structure 710 and the p– single crystalline silicon structure 712 from the p-doped glass 736 and the n-doped glass 732 respectively. The n+ and p+ polysilicon gate layers, 763 and 764 respectively, are directionally etched to leave only on the vertical side walls of the NMOS and PMOS device regions, 707 and 705. This step forms heavily doped first and second n+ gates,

763A and 763B, in the NMOS device region 707, opposite opposing sidewall surfaces, 765A and 765B respectively. Likewise, the directional etch forms heavily doped p+ silicon gates, 764A and 764B, in the PMOS device region 705, opposite opposing sidewall surfaces, 766A and 766B respectively. The structure is then as appears in Figure 6M.

Figure 6N provides a broader perspective view following the preceding series of process steps. Figure 6N illustrates full length NMOS and PMOS devices, 770 and 771 respectively. Figure 6N illustrates the location of the newly formed first source/drain regions, 781 and 782, as well as the second source/drain regions, 783 and 784, for the NMOS and PMOS devices, 770 and 771. Figure 6O is a top view of Figure 6N taken along cut line 6N-6N.

Finally, in a final sequence of processing steps, and following conventional method, a photoresist is applied and masked to expose any vertical walls where polysilicon 763 or 764 is to be removed to terminate gate lines. Such polysilicon 763 or 764 is then etched back by any suitable method, such as by RIE. The photoresist is stripped using conventional photoresist stripping techniques. An oxide or other insulator is deposited and planarized to fill the trenches 714 between the NMOS and PMOS devices, 770 and 771 respectively. The insulator deposition is performed by any suitable method, such as by CVD. The planarization is also achieved by any suitable technique, such as by CMP.

Contact holes and wiring for both the gate-contact and the electrical contact are formed through conventional processing steps in order to complete integrated circuit formation. One skilled in the art will recognize the method to these steps and, hence, they are not disclosed as part of this application.

Figure 7 is a perspective view of an array of transistors, 412a, 412b, 412c, 412d, 412e, and 412f, formed according to the method provided in Figures 4A-4K and Figures 5A-5C. Each MOSFET in the array of transistors, 412a, 412b, 412c, 412d, 412e, and 412f, is vertically formed on a substrate 510. In one embodiment, substrate 510 is a p-type bulk silicon substrate. In another embodiment, the substrate 510 includes an insulator layer 902. Each transistor, 412a, 412b, 412c, 412d, 412e, and 412f, includes a first conductivity type, first source/drain region 512, a second conductivity type, body region 514, and a first conductivity type, second source/drain region 516. In one embodiment, the first source/drain region is formed by ion implantation of a p-type dopant into the substrate 510. Another embodiment, includes forming

the first source/drain region 512 by vertically growing a p-type epitaxial layer from the substrate 510. In an alternate embodiment, the first source/drain region 512 is formed by vertically growing an n-type epitaxial layer from the substrate 510. In still another embodiment, the first source/drain region 512 is formed by first ion implanting a dopant into the substrate and then vertically growing an epitaxial layer. Each body region 514 has opposing sidewall surfaces and is vertically formed on the first source/drain region 512 by vertically growing an epitaxial layer according to the method provided Figures 4A-4K and Figures 5A-5C. Each second source/drain region 516 is formed on the vertical body region 514 in an identical manner to the first source/drain region 516. Each body region 514 is formed sufficiently thin, vis-a-vis the doping concentration, such that the body region 514 can be fully depleted when a potential is applied to the body region 514.

Focusing on transistors 412b and 412e, Figure 7 illustrates a first gate 506A provided in trench 521. The first gate 506A opposes a first one 519A of the opposing sidewall surfaces, 519A and 519B, for the body regions 514 of transistors 512b and 512e. In Figure 7, a second gate 508B is provided in trench 522. The second gate 508B opposes a second one 519B of the opposing sidewall surfaces, 519A and 519B, for the body regions 514 of transistors 412b and 412e. Fully depleting the body regions 514 is controlled by the synchronous bias of the first and second gates, 506A and 508B. In one embodiment, the first gate 506A and second gate 508B are independently operable and can be biased from separate sources. In an alternative embodiment, the first gate 506A and second gate 508B are biased from a single source.

Focusing on transistors 412a and 412d, a first gate 506B is provided in trench 521. The first gate 506B opposes a first one 519C of the opposing sidewall surfaces, 519C and 519D, for transistors 412a and 412d. First gates 506A and 506B are independent and electrically isolated from one another.

Figure 8 is a perspective view of a MOSFET 401 formed according to the method provided in Figures 6A-6N. The MOSFET 401 represents either an n-channel MOSFET (NMOS), or a p-channel MOSFET (PMOS) depending on a selected doping profile as will be understood by one of ordinary skill in the art of semiconductor fabrication. The MOSFET 401 includes a vertically formed body region 411 that extends outwardly from a substrate 405 of p– silicon material. In one embodiment, the body region 411 is formed on an insulator layer 490

formed on the substrate 405. The body region 411 has an upper surface 470 and opposing sidewall surfaces, 481 and 482 respectively. The body region 411 is formed sufficiently thin, vis-a-vis the doping concentration, such that the body region 411 can be fully depleted when a potential is applied to the body region 411. In the PMOS embodiment, the body region 411 is formed of a p– silicon material. In the NMOS embodiment, the body region 411 is formed of an n– silicon material.

A first source/drain region 416A is formed adjacent to the upper surface 470 and the opposing sidewall surfaces, 481 and 482, of the body region 411. Forming the first source/drain region 416A adjacent to the body region 411 includes encasing a portion of the body region 411 with a doped glass layer 426. In the NMOS embodiment, the doped glass layer 426 can be either an Arsenic silicate glass (ASG), or phosphorus silicate glass (PSG). The doped glass layer 426 is deposited by chemical vapor deposition (CVD) and then annealed to form the n-type layer of doped silicon material on the body region 411. In the PMOS embodiment, forming the first source/drain region 416A adjacent to the body region 411 includes encasing a portion of the body region 411 with a doped glass layer 426 of Borosilicate glass (BSG). The BSG is deposited by CVD and then annealed to form the p-type layer of doped silicon material on the body region 411.

Similarly, a second source/drain region 416B is formed adjacent to the upper surface 470 and the opposing sidewall surfaces, 481 and 482, of the body region 411. The second source/drain region 416B is formed in a fashion which appropriately accords to forming the first source/drain region 416A, as will be understood by one of ordinary skill in the art of semiconductor fabrication. The MOSFET 401 further includes a gate oxide layer 429 located on the opposing sidewalls, 481 and 482. A first gate 466 is formed on the gate oxide 429 on a first one 481 of the opposing sidewalls surfaces, 481 and 482, of the body region 411. A second gate 467 is formed on the gate oxide 429 on a second one 482 of the opposing sidewalls surfaces, 481 and 482, of the body region 411. The oxide layer 429 and the first and second gates, 466 and 467 respectively, are formed according to the method taught in connection with Figures 6A-6N.

Figure 9 is a planar view of an embodiment of a transistor according to the teachings of the present invention. Figure 9 illustrates a dual gated transistor 900. The dual gated transistor has a first source/drain region 924A, a body region 926, and a second source/drain region 924B.

The body region 926 has opposing sidewall surfaces, 941 and 940 respectively, and the body region 926 includes a fully depleted structure. A first gate 920 is located on a first one 941 of the opposing sidewall surfaces, 941 and 940 respectively. A second gate 922 is located on a second one 940 of the opposing sidewall surfaces, 941 and 940 respectively. The threshold voltage (Vt) for the dual-gated transistor 900 is not dependent on bulk charge in the body region 926. This feature, or aspect, of the present invention is best understood by comparing the following equations and schematic representations with Figure 9.

The threshold voltage for a conventional MOSFET is given by Equation 1,

$$VT = \left|2\Phi_f\right| + \left|QB/Cox\right| \quad (1)$$

where QB = q NA Wd, and is the relatively large bulk charge in the surface depletion or space charge region. For simplicity, this equation assumes an idealized structure with no oxide charge or work function differences. Note that the threshold voltage (Vt) depends directly on the magnitude of the term, QB/Cox. This term is significant and normally is of the same order of magnitude as the first term, $2\phi_f$. Fluctuations in QB will result in fluctuations of the threshold voltage (Vt). This is not the case for the fully depleted dual gated structure in Figure 9.

The following equations outline the same type of calculation for the threshold voltage (Vt) of a fully depleted dual gated structure. In the fully depleted dual-gated structure,

$$VT = \left|2\Phi_f\right| + \left[\left|QB\right| + \frac{Esi\ Eox\left(\left|2\Phi_f\right| - VBG - \left|QB/2Csi\right|\right)}{\left(Esi\ tox + Eox\ tsi\right)}\right] / Cox \quad (2)$$

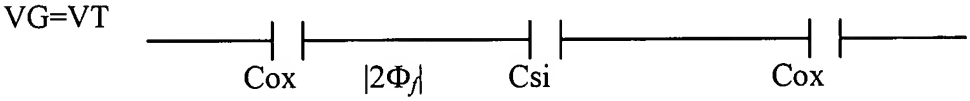
This equation again assumes an idealized structure with no oxide charge or work function differences. Note that in Equation 2, the threshold voltage can now be controlled by the backgate bias voltage, VBG. A negative bias on the backgate will increase the front gate threshold voltage (Vt). Note also that if QB is small, the doping, NA, is low and/or the thickness, tsi, is small, then (Vt) does not depend strongly on QB. Equation 2 can also be written,

$$VT = |2\Phi_f| + \left[|QB| + \frac{Csi\ Cos\left[|2\Phi_f| - VBG - |QB/2Csi|\right]}{(Csi + Cos)} \right] / Cox \quad (3)$$

In the limiting case as QB approaches zero then,

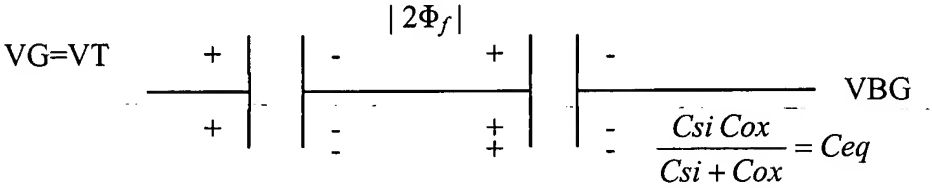
$$VT = |2\Phi_f| + \frac{Csi}{Csi + Cox}\left(|2\Phi_f| - VBG\right) \quad (4)$$

This equation just represents three capacitors in series, the front gate oxide 921, the capacitance of the silicon body region 926, and the backgate oxide 923, as illustrated below;



(5)

and this can be reduced to two capacitors in series;



(6)

and then the charge, QBD, found on these two capacitors.

$$QBD = \left(|2\Phi_f| - VBG\right)Ceq \quad (7)$$

One can then calculate the voltage drop across the front gate oxide 621, $\Delta V = QBD/Cox$,

$$\Delta V = \frac{Csi}{Csi + Cox}\left(|2\Phi_f| - VBG\right) \quad (8)$$

and finally the gate voltage (Vt) at threshold for the front gate.

$$VT = VG = \left|2\Phi_f\right| + \frac{Csi}{Csi + Cox}\left(\left|2\Phi_f\right| - VBG\right) \tag{9}$$

b2

In this limiting case, the threshold voltage (Vt) depends only on the thickness of the oxides, 921 and 923, and silicon body region 926 and not at all on the bulk charge. It becomes apparent in this case that the threshold voltage (Vt) can be made insensitive to fluctuations in dopant atom concentrations. The threshold voltage (Vt) is controlled by the backgate voltage, VBG, which can be accurately set.

An improved method and structure are provided for MOSFETs which reduce or eliminate the effects of statistical dopant fluctuations. The structure includes a dual-gated FET which can be fabricated according to a novel processing sequence, but uses current fabrication line CMOS processing tools and process techniques. Hence the invention does not require any additional masks, forms, or an increase in the number of process steps. The dual-gated MOSFET has two gates one on each side of a thin fully depleted silicon structure, or body region. The small volume, or thin width, of the body of the dual-gated transistor allows the device to be fully depleted in MOSFET operation. In effect, the bulk charge in the body region is extremely small, negligible in device operation, and therefore the threshold voltage (V_t) does not depend on statistical fluctuations in dopant atom concentrations. The improved method and structure facilitate a future generation of sub 0.5 μm, uniform, and low threshold voltage (V_t) devices. The improved method and structure additionally facilitate an increased range of applications for sub-0.5 μm MOSFETs which include use in producing drivers and clock drivers with uniform characteristics and delays.